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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,507	HISAMOTO ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/4/3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 5-11, and 13-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaya et al. (U.S. Patent No. 5,821,581).

In re claims 1, 9 and 19-21, Kaya discloses a semiconductor device, comprising:

a semiconductor substrate (10);

first and second semiconductor regions (12, 14) of a first conductivity type formed in said semiconductor substrate;

a first channel region (16b) and a second channel region (16a) between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate (22) formed above said first channel region via a first insulator (26); and

a second gate (20) formed above said second channel region via a second insulator (20);

wherein writing and erasing operations are performed by injecting charge into said second insulator (column 4, lines 11-22); and

the charge density of an impurity in said first channel region is different from the charge density of an impurity in said second channel region (column 3, lines 58-65), wherein the charge density is set within the range 10E 17 to 10E 18.

In re claims 2 and 13, Kaya discloses the devices of claims 1 and 9 respectively, wherein the charge density of an impurity in said second channel region (16a) is lower than the charge density of an impurity in said second channel region (16b; column 3, lines 58-65).

In re claim 5, Kaya discloses the device of claim 1, wherein the thickness of said second insulator (18 + 20) is larger than a thickness of said first insulator (26).

In re claims 7 and 14, Kaya discloses the devices of claims 1 and 9 respectively, wherein said second gate is adjacent to said first gate via said second insulator.

In re claim 8, Kaya discloses the device of claim 1. The limitation, "... is performed by ... insulator" is a recitation of the intended use of the claimed device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 18, Kaya discloses the device of claim 17. The limitations of claim 17 and 18 regarding applying voltage pulses are recitations of the intended use of the device that do not further limit the claimed structure.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Mihnea et al> (U.S. Patent No. 6,449,189 B2).

In re claim 1, Minhea (esp. Fig. 1) discloses a semiconductor device, comprising:

a semiconductor substrate (106);

first and second semiconductor regions (133, 124) of a first conductivity type formed in said semiconductor substrate;

a first channel region (137) and a second channel region (127) between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate (148) formed above said first channel region via a first insulator (145); and

a second gate (154) formed above said second channel region via a second insulator (151);

wherein writing and erasing operations are performed by injecting charge into said second insulator; and

the charge density of an impurity in said first channel region is different from the charge density of an impurity in said second channel region

In re claim 3, Mihnea discloses the device of claim 1, wherein the impurity of a second conductivity type opposite to said first conductivity type is introduced into said first channel region (127), and the impurity of the first conductivity type and the impurity of the second conductivity type are introduced into the second channel region (136, 137).

Claim Rejections - 35 USC § 103

4. Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaya as applied to claims 1 and 9 above, and further in view of Ogura et al. (U.S. Patent No. 6,388,293 B1).

In re claims 4 and 12, Kaya discloses the devices of claims 1 and 9 respectively, wherein said second insulator comprises a two layer oxide-nitride layer but does not expressly disclose a three-layer ONO layer. Ogura discloses a three-layer ONO layer. It would have been obvious for one skilled in the art at the time of the invention to use a three layer ONO layer as disclosed by Ogura in the device of Kaya for the purpose, for example, of enhancing the charge accumulation capabilities of the device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815